In the Claims:

The following version of the claims replaces all other previously presented versions.

1. (Presently Amended) An analog-to-digital converter for use in an image sensor, comprising:

a storage means for storing a digital image data and outputting the digital image data to a bit line; and

an acceleration means for detecting a voltage variation of the bit line to accelerate the voltage variation of the bit line,

wherein the acceleration means includes

a first means, coupled to a node, for detecting the voltage variation of the bit line;

a second means, in response to an inverted precharge signal, for determining a voltage level of the node; and

a third means, responsive to the voltage level of the node, for electrically coupling the bit line to the ground.

2. (Original) The analog-to-digital converter as recited in claim 1, further comprising:

a precharge means for precharging the bit line in response to a precharge signal.

3. (Canceled)

4. (Presently Amended) The analog-to-digital converter as recited in claim ~~3~~1, wherein the first means is a PMOS transistor, which has a source coupled to a power voltage level, a gate coupled to the bit line, and a drain coupled to the node.

5. (Original) The analog-to-digital converter as recited in claim 4, wherein the second means is an NMOS transistor, which has a drain coupled to the node, a source coupled to the ground, and a gate receiving the inverted precharge signal.

6. (Original) The analog-to-digital converter as recited in claim 5, wherein the third means is an NMOS transistor, which has a drain coupled to the bit line, a source coupled to the ground, and a gate receiving the voltage level of the node.

7. (Presently Amended) An image sensor comprising:

a pixel array for sensing light beam to generate an analog image data;

a control and interface means for managing an interface with external circuits and generating control signals, the control signals including a digital count signal, a column address signal, and a bank selection signal;

a decoding means for decoding the column address signal to generate a column selection signal; and

a conversion means for converting the analog image data into a digital image data, the conversion means including[[:]]

a ramp voltage generation means for generating a ramp voltage signal whose voltage level is linearly decreased according to a clock;

a comparison means for comparing a voltage level of the ramp voltage signal with that of the analog image data to generate a latch enable signal;

a storage means for storing the digital count signal in response to the latch enable signal and the bank selection signal and outputting stored digital count signal to a bit line in response to the column selection signal; and

an acceleration means for detecting a voltage variation of the bit line to accelerate the voltage variation of the bit line,

the acceleration means including

a first means, coupled to a node, for detecting the voltage variation of the bit line;

a second means, in response to an inverted precharge signal, for determining a voltage level of the node; and

a third means, responsive to the voltage level of the node, for electrically coupling the bit line to the ground.

8. (Original) The image sensor as recited in claim 7, further comprising a precharge means for precharging the bit line in response to a precharge signal.

9. (Canceled)

10. (Presently Amended) The image sensor as recited in claim 97, wherein the first means is a PMOS transistor, which has a source coupled to a power voltage level, a gate coupled to the bit line, and a drain coupled to the node.

11. (Original) The image sensor as recited in claim 10, wherein the second means is an NMOS transistor, which has a drain coupled to the node, a source coupled to the ground, and a gate receiving the inverted precharge signal.

12. (Original) The image sensor as recited in claim 11, wherein the third means is an NMOS transistor, which has a drain coupled to the bit line, a source coupled to the ground, and a gate receiving the voltage level of the node.

13. (Original) The image sensor as recited in claim 7, wherein the pixel array includes a plurality of unit pixels, arranged in a matrix of MxN, M and N being integers, each unit pixel having a photodiode for sensing the light beam to generate photoelectric charges and four NMOS transistors for outputting the analog image data corresponding to the photoelectric charges.

14. (Original) The image sensor as recited in claim 8, wherein the latch enable signal is activated to a high level while the voltage level of the ramp voltage signal is higher than that of the analog image data.

15. (Original) The image sensor as recited in claim 14, wherein the storage means includes:

a first NMOS transistor having a drain coupled to the digital count signal and a gate receiving the latch enable signal;

a second NMOS transistor having a drain coupled to a source of the first NMOS transistor and a gate receiving the bank selection signal;

a third NMOS transistor having a source coupled to a ground and a gate receiving the digital count signal transferred via the first and the second NMOS transistors; and

a fourth NMOS transistor having a drain coupled to the bit line, a source coupled to a drain of the third NMOS transistor, and a gate receiving the column selection signal.

16. (Original) The image sensor as recited in claim 15, wherein a phase of the clock is equal to that of the precharge signal.